

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT241** Octal buffer/line driver; 3-state

Product specification  
File under Integrated Circuits, IC06

September 1993

## Octal buffer/line driver; 3-state

## 74HC/HCT241

## FEATURES

- Output capability: bus driver
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT241 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT241 are octal non-inverting buffer/line drivers with 3-state outputs. The 3-state outputs are controlled by the output enable inputs  $\overline{OE}$  and  $OE$ .

## QUICK REFERENCE DATA

$GND = 0 \text{ V}$ ;  $T_{amb} = 25 \text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6 \text{ ns}$

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>	$C_L = 15 \text{ pF}$ ; $V_{CC} = 5 \text{ V}$	7	11	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{PD}$	power dissipation capacitance per buffer	notes 1 and 2	30	30	pF

## Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = GND$  to  $V_{CC}$

For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5 \text{ V}$

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	$\overline{1OE}$	output enable input (active LOW)
2, 4, 6, 8	$1A_0$ to $1A_3$	data inputs
3, 5, 7, 9	$2Y_0$ to $2Y_3$	bus outputs
10	GND	ground (0 V)
17, 15, 13, 11	$2A_0$ to $2A_3$	data inputs
18, 16, 14, 12	$1Y_0$ to $1Y_3$	bus outputs
19	$2OE$	output enable input (active HIGH)
20	$V_{CC}$	positive supply voltage

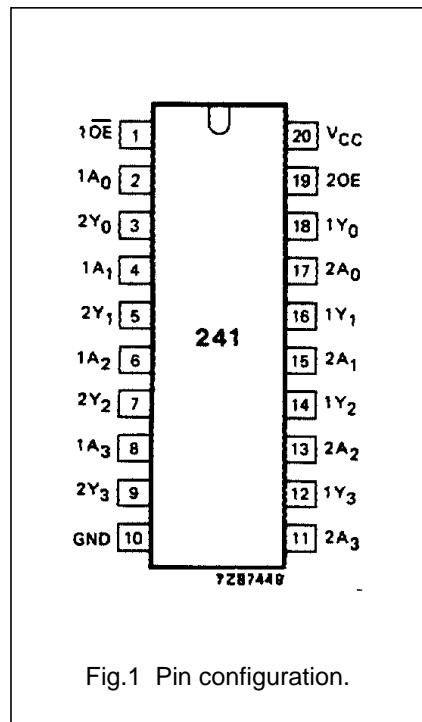


Fig.1 Pin configuration.

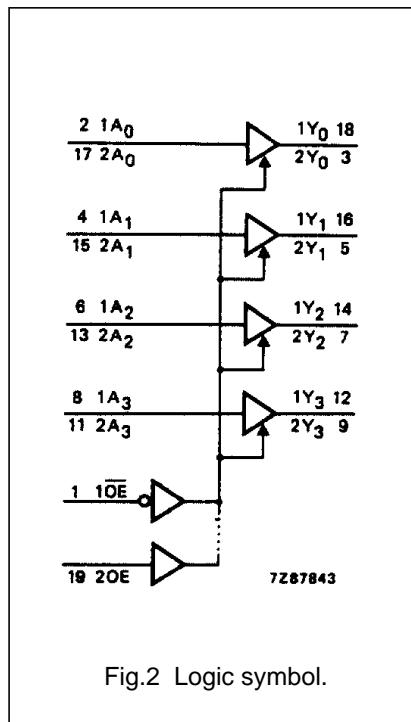


Fig.2 Logic symbol.

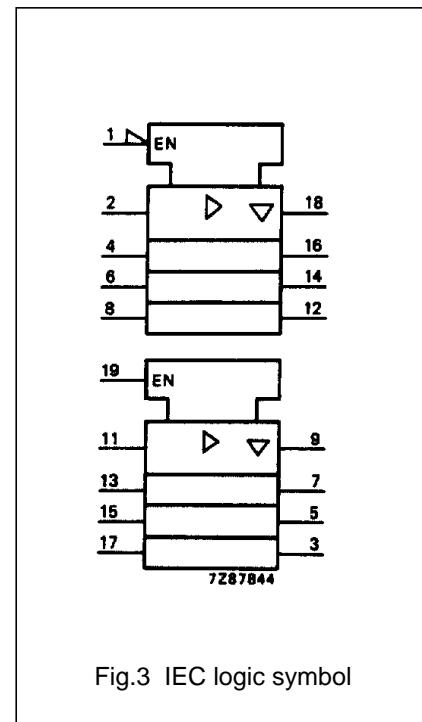


Fig.3 IEC logic symbol

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## FUNCTION TABLES

INPUTS		OUTPUT
$1\bar{OE}$	$1A_n$	$1Y_n$
L	L	L
L	H	H
H	X	Z

INPUTS		OUTPUT
$2\bar{OE}$	$2A_n$	$2Y_n$
H	L	L
H	H	H
L	X	Z

## Note

1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- Z = high impedance OFF-state

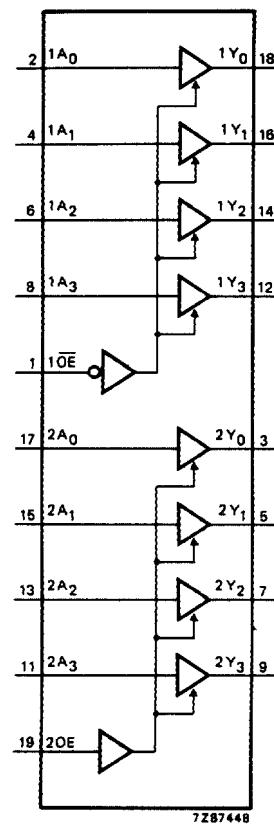


Fig.4 Functional diagram.

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: bus driver

$I_{CC}$  category: MSI

## AC CHARACTERISTICS FOR 74HC

$GND = 0 \text{ V}$ ;  $t_r = t_f = 6 \text{ ns}$ ;  $C_L = 50 \text{ pF}$

SYMBOL	PARAMETER	$T_{amb} (\text{ }^{\circ}\text{C})$						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	WAVEFORMS		
		+25			-40 to +85		-40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>	25 9 7	100 20 17		125 25 21		150 30 26	ns	2.0 4.5 6.0	Fig.5		
$t_{PZH}/t_{PZL}$	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>	30 11 9	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6		
$t_{PHZ}/t_{PLZ}$	3-state output disable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>	39 14 11	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6		
$t_{THL}/t_{TLH}$	output transition time	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5		

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
1A <sub>n</sub>	0.70
2A <sub>n</sub>	0.70
1OE	0.70
2OE	1.50

## AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HCT							V <sub>CC</sub> (V)	WAVEFORMS		
		+25		-40 to +85		-40 to +125						
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay 1A <sub>n</sub> to 1Y <sub>n</sub> ; 2A <sub>n</sub> to 2Y <sub>n</sub>		13	22		28		33	ns	4.5	Fig.5	
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		15	30		38		45	ns	4.5	Fig.6	
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time 1OE to 1Y <sub>n</sub> ; 2OE to 2Y <sub>n</sub>		18	30		38		45	ns	4.5	Fig.6	
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time		5	12		15		18	ns	4.5	Fig.5	

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## AC WAVEFORMS

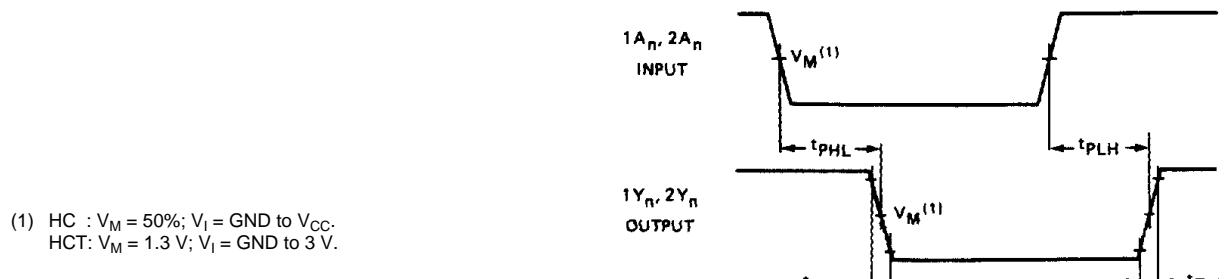


Fig.5 Waveforms showing the input ( $1A_n, 2A_n$ ) to output ( $1Y_n, 2Y_n$ ) propagation delays and the output transition times.

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

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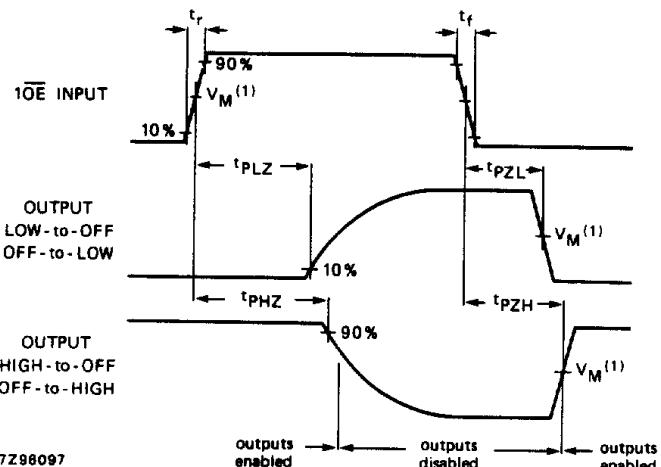


Fig.6 Waveform showing the 3-state enable and disable times for input  $1\overline{OE}$ .

(1) HC :  $V_M = 50\%$ ;  $V_I = \text{GND to } V_{CC}$ .  
 HCT:  $V_M = 1.3 \text{ V}$ ;  $V_I = \text{GND to } 3 \text{ V}$ .

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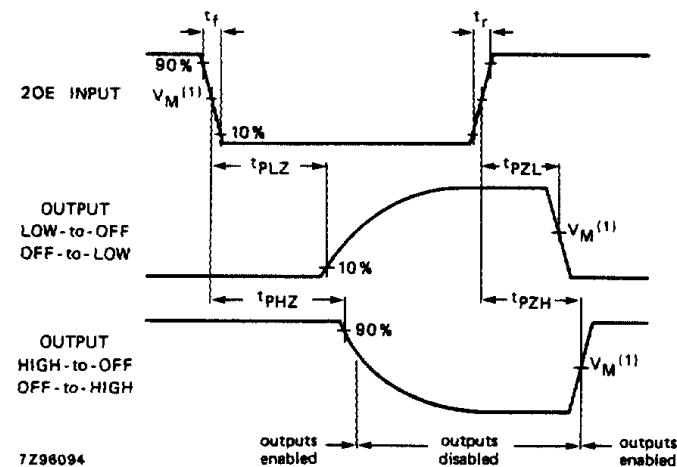


Fig.7 Waveform showing the 3-state enable and disable times for input  $2\overline{OE}$ .

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**PACKAGE OUTLINES**See "*74HC/HCT/HCU/HCMOS Logic Package Outlines*".